Amendments to the Specification

[0018] Figure 6 illustrates the four partial response signal levels depicted in Figure 5 relative to a common mode level, L_{CM}. In the case of a differential signaling system, the partial response to the preceding symbol may be viewed as increasing or decreasing the differential amplitude (i.e., the amplitude difference between the signals that form the differential signal pair) relative to a nominal differential amplitude. Normalizing the positive and negative signal levels for the nominal differential amplitude to 1 and -1, respectively, the common mode level, L_{CM}, becomes zero, and the four possible signal levels become $1+\alpha$, $1-\alpha$, $-1+\alpha$ and $-1-\alpha$, where α represents the magnitude of the partial response to the preceding symbol. Thus, when the preceding symbol, D_{N-1}, is a '0', the incoming symbol, D_N, is represented by a signal level at either $1-\alpha$ or $-1-\alpha$, depending on whether D_N is a '1' or '0'. Similarly, when $D_{N-1}= 1$, the incoming symbol is represented by a signal level at either $1+\alpha$ or $-1+\alpha$ according to the state of the current symbol. In the former case (i.e., when $D_{N-1}=0$), the two complementary signal levels, $-1-\alpha$ and ~~$1-\alpha$~~ $1-\alpha$, have a common mode of $-\alpha$, as shown in box 151. In the latter case (i.e., when $D_{N-1}=1$), the two complementary signal levels, $1+\alpha$ and $-1+\alpha$, have a common mode of $+\alpha$, as shown in box 153.

[0019] Figure 7 illustrates a partial response receive circuit 200 according to an embodiment of the invention that exploits the bi-modal characteristic of the signal levels depicted in Figures 5 and 6. The partial response circuitry

includes a compare circuit 202 to sample the input data signal, D_N, and a decision circuit 204 to generate an output data value (i.e., received data value) based on data samples generated by the compare circuit 202. Rather than a single comparator that distinguishes between binary signaling levels based on whether the sampled signal is above or below a common mode threshold, the compare circuit 202 includes two comparators 201 and 203 having threshold levels that are offset from the common mode threshold by the two possible partial responses to the preceding symbol. That is, the threshold level of the comparator 201 is set the $+\alpha$ level, and the threshold level of the comparator 203 is set to the $-\alpha$ level. By this arrangement, if the preceding symbol was a '1' (i.e., $D_{N-1}=1$), the comparator 201 will resolve the incoming signal as being a '1' or '0' by determining whether the signal level is above or below the partial response level, $+\alpha$. Conversely, if $D_{N-1}=0$, the comparator 203 will resolve the incoming signal as being a '1' or '0' by determining whether the signal is above or below the partial response level, $-\alpha$. Because both comparisons are performed for each incoming symbol, the selection of which comparator output represents the state of the symbol may be delayed until the state of the preceding symbol is resolved. In the partial response receive circuit 200, for example, the sample values output by the comparators 201 and 203 are output to the decision circuit 204 where they are optionally stored in storage elements 208 and 209 (e.g., D flip-flops or other types of storage circuits) and provided to respective input ports of a select circuit 205 (e.g., a multiplexer). The sample value selected by the select circuit 205 is stored in a storage circuit 207 in

response to a sampling clock signal 210 (or other timing control signal) at which point the sample value becomes the ~~D_{N-1}~~ $\underline{D_{N-1}}$ sample value. The D_{N-1} sample value stored within storage circuit 207 is fed back to the select input of the select circuit 205 to select one of the two sample values generated by the comparators 201 and 203. That is, the D_{N-1} sample value is used to select, via select circuit 205, which of the comparators 201 and 203 will source the D_N sample. In an embodiment that includes the storage elements 208 and 209, the output of storage circuit 207 becomes the D_{N-2} sample value and is used to select one of the D_{N-1} sample values output from the storage elements 208 and 209.

[0023] Figure 9 illustrates a partial response receive circuit 215 for use in a double data rate signaling system. The partial response receive circuit 215 includes an odd-phase receive circuit 216 clocked by an odd-phase sampling clock signal 210_O ($SCLK_O$), and an even-phase receive circuit 217 clocked by an even-phase sampling clock signal 210_E ($SCLK_E$). The odd- and even-phase receive circuits 216, 217 are similar to the partial response receive circuit 200 of Figure 7, except that, due to the interleaved nature of the samples they generate, the select circuit 225 of the odd-phase receive circuit 216 is controlled by a latched instance of a sample selected by the select circuit 239 in the even-phase receive circuit 217 and, conversely, the select circuit 239 of the even-phase receive circuit 217 is controlled by a latched instance of a sample selected by the select circuit 225 in the odd-phase receive circuit 216. Samples D_N^+/D_N^- are generated by comparators 232 and 233, stored in storage circuits 235 and

237, and then selected by select circuit 239 to form the even-phase pipeline (EVEN PIPE) illustrated in Figure 10 (the output of the select circuit 239 optionally being buffered in storage circuit 243 in response to the even-phase sampling clock signal 210_E). Similarly, samples D_{N+1}^{+}/D_{N+1}^{-} are generated by comparators 218 and 219, stored in storage circuits 221 and 223, then selected by the select circuit 225 to form the odd-phase pipeline (ODD PIPE) illustrated in Figure 10 (the output of the select circuit 225 optionally being buffered in storage circuit 227 in response to the odd-phase sampling clock signal 210_O). Thus, when an odd phase sample D_{N-1} is selected by select circuit 225, the D_{N-1} sample is latched within latch element 241 of the even-phase receive circuit (thereby making D_{N-1} available for a full cycle of the even-phase clock signal 210_E) and thereafter used to select the subsequent even-phase sample D_N. The selected even phase sample D_N is then latched within latch element 228 of the odd-phase receiver and thereafter used to select the subsequent odd-phase sample, D_{N+1}. For higher data rates, the number of partial-cycle receive circuits (circuits 216 and 217 each being a half-cycle receive circuit) may be increased according to the data rate. For example, in a quad data rate system, a partial response receiver includes four quarter-cycle receive circuits interconnected such that sample N within a first quarter-phase receive circuit is used to select sample N+1 within a second quarter-phase receive circuit; sample N+1 within the second quarter-phase receive circuit is used to select sample N+2 in a third quarter-phase receive circuit; sample N+2 is used to select sample N+3 in a fourth quarter-phase receive circuit; sample N+3 is used to select sample N+4 in the first quarter

phase receiver; and so forth. In the remainder of this description, various partial response receive circuit embodiments are described in the context of a single data rate (SDR) signaling system. Each of the embodiments disclosed may be modified as described in reference to Figures 8-10 to support multi-data rate signaling.

[0028] Figure 12 illustrates a signaling system 300 according to an embodiment of the invention. The signaling system 300 includes a transmit device 301 and receive device 309 that employ embedded scoping to determine partial response amplitudes. The transmit device 301 includes a pattern generator 303, data selector 305, equalizing transmitter 307 and application logic 302. The application logic 302 performs the core function of the transmitting device (e.g., signal processing, instruction processing, routing control, or any other function) and provides transmit data (TX DATA) to a first input of the data selector 305. During normal operation, the application logic 302 outputs a logic low scope signal 306 (SCOPE) to the data selector 305 to select the transmit data to be passed to the equalizing transmitter 307 for transmission to the receive device 309 via signal path 122 (which may include or be connected to numerous sources of discontinuity such as connectors, vias, stubs, etc.). During a scoping mode of operation, the application logic 302 drives the scope signal 306 high to enable a scoping mode of operation within the transmit device 301. In the scoping mode, the data selector 305 selects a repeating single-symbol pulse sequence (e.g., a test signal such as: 00100…00100...00100…) generated by the pattern generator 303

to be transmitted to the receive device 309. The receive device 309 includes a partial response receiver 310 to receive the incoming data signal, a pattern register 311 to store a local version of the single-symbol pulse sequence, a multiplexer 312 to enable the pattern register 311 to be switched between load and barrel-shifting modes, [[a]] an XOR gate 313 to compare the received data sequence with the locally generated sequence, and application logic 315 (or other logic) to generate a threshold voltage adjust signal (THRESH ADJ) to step the threshold voltage used within the partial response receive circuit through their scoping ranges. In [[on]] one embodiment, the thresholds applied to the multiple comparators of the partial response receive circuit are set to the same nominal starting value and stepped together for purposes of embedded scoping. In an alternative embodiment, only one comparator of the partial response receive circuit is used when scoping mode is enabled. The application logic may additionally generate a clock adjust signal (not shown) to step the sampling clock through a sequence of phase offsets within a cycle of the sampling clock signal. The application logic 315 additionally builds a trace record (i.e., data indicative of the incoming data sequence) based on the output of XOR gate 313.

[0030] Figure 13 illustrates a sample waveform trace 320 of a pulse response captured by an embedded scope within the signaling system of Figure 12. As shown, the waveform starts and ends at a steady-state low level which corresponds to the $-1-\alpha$ level discussed in reference to Figures 5 and 6. A pulse (i.e., D=1) is received at time T3, and the partial response

of the pulse is received at time T4. Due to the preceding zero-valued symbol, the signal level sampled at time T3 corresponds to the $1-\alpha$ level. Similarly, due to the preceding one-valued symbol, the signal level sampled at time T4 corresponds to the $-1+\alpha$ level. The difference between the [[$-1+\alpha$]] $\underline{-1+\alpha}$ level and the $-1-\alpha$ level may be determined by the application logic 315 of Figure 12 (or other circuitry) and used to determine $\pm\alpha$. That is, $\alpha = ((-1+\alpha)-(-1-\alpha))/2$. The normalized signal level, 1, may be used in certain clock recovery operations (discussed below) and may be determined from the pulse level and the steady-state low level (i.e., $1=((1-\alpha)-(-1-\alpha))/2$). Once determined, the α level may be applied to the comparators of the partial response receive circuit to enable partial response operation.

[0037] Figure 16 illustrates an alternative circuit arrangement 375 that may be used in place of the averaging circuits 361 and 365 of Figure 15. Instead of averaging the $C_{1+\alpha}$ and $C_{-1+\alpha}$ count values to generate the $C_{+\alpha}$ value, $C_{+\alpha}$ is generated by halving the difference between the $C_{1+\alpha}$ and the [[$C_{1-\alpha}$]] $\underline{C_{1-\alpha}}$ control values (i.e., $C_\alpha = ((C_{1+\alpha})-(C_{1-\alpha}))/2$). Similarly, the $C_{-\alpha}$ value is generated by halving the difference between the [[$C_{-1-\alpha}$]] $\underline{C_{-1-\alpha}}$ and the $C_{-1+\alpha}$ control values. Thus, the circuit of Figure 16 includes a difference circuit 376 to generate 2α by subtracting the $C_{1-\alpha}$ control value from the $C_{1+\alpha}$ control value, and a divide-by-2 element 377 (which may be a implemented by dropping the least significant bit of the difference) to generate C_α by halving the 2α value. Difference circuit 379 and divide-by-2 element 380 are used in a similar manner to generate $C_{-\alpha}$ from count values $C_{-1+\alpha}$ and $C_{-1-\alpha}$ in a corresponding manner.

[0040] The sampling circuit 425 includes a differential amplifier 426 formed by transistors 423 and 424, a sense amplifier 427 formed by back-to-back coupled inverters 428 and 429, and a storage circuit 436 formed by a set-reset flip-flop. The differential amplifier 426 includes control inputs coupled to the output nodes 418 and 419, respectively, of the preamplifier 401, and output nodes 431 and 433 coupled to source terminals of the inverters 428 and 429, respectively. [[.]] A biasing transistor 430, switchably controlled by the sampling clock signal 210 (or other sample control signal), is coupled between the differential amplifier 426 and a ground reference (or other low voltage reference). The sampling clock signal 210 is additionally coupled to control inputs of positively doped MOS (PMOS) transistors 434 and 435 which are coupled between a supply voltage (e.g., V_{DD}) and output nodes of the inverters 428 and 429. By this arrangement, when the sample clock signal 210 is low, transistor 430 is switched off, and transistors 434 and 435 are switched on to pre-charge the output nodes of the inverters 428 and 429 to the supply voltage. The output nodes of the inverters 428 and 429 are coupled to active-low set and reset inputs, respectively, of the storage circuit 436, so that the content of the storage circuit 436 is maintained through the low half-cycle of the sample clock signal 210. When the sample clock signal 210 goes high, biasing transistor 430 is switched on and draws current through the two transistors 424 and 423 of the differential amplifier 426 in proportion to the voltages developed on the output nodes 418 and 419 of the preamplifier 401. Thus, if the voltage developed on node 419 is higher

than the voltage on node 418, the current drawn by biasing transistor 430 will flow primarily through transistor 423. Conversely, if the voltage developed on node 418 is higher than the voltage on 419, the current drawn by biasing transistor will flow primarily through transistor 423. Transistors 434 and 435 are switched off in response to the high-going sample clock signal 210, so that the pre-charged outputs of the inverters 428 and 429 are discharged by currents flowing through transistors 423 and 424. By this operation, if the incoming signal (D) exceeds the common mode voltage, ((D+ /D) divided by 2), by more than the +α threshold level (i.e., the incoming signal exceeds the +α threshold level), the current drawn by biasing transistor 430 will flow primarily through transistor 423. Consequently, the output node of inverter 429 will be discharged more rapidly than the output node of inverter 428, driving the output of inverter 429 low and driving the output of inverter 428 high (i.e., the PMOS transistor within inverter 428 is switched on and the NMOS transistor within inverter 428 is switched off). The low output of inverter 429 is applied to the active-low set input of the storage circuit 436, causing the storage circuit 436 to store a logic '1' sampled data value. By contrast, if the incoming signal level does not exceed the +α threshold level, the current drawn by biasing transistor 430 will flow primarily through transistor 424, thereby driving inverter 428 low (and driving inverter 429 high) to store a logic '0' sampled data value within storage circuit 436.

[0041] Figure 18 illustrates an embodiment of the current DAC 411 of Figure 17. The current DAC 411 includes control

transistors 437_0-437_{N-1} and biasing transistors 439_0-439_{N-1}. Each of the control transistors 437_0-437_{N-1} is coupled in series (e.g., source to drain) with a corresponding one of the biasing transistors 439_0-439_{N-1} to form a transistor pair that is coupled between a reference voltage (ground in this example) and an output node 438 (i.e., the node to be connected to the source terminals of the transistors which form the differential amplifier 402). Gate terminals of the control transistors 437_0-437_{N-1} are coupled to receive respective component signals, $C_\alpha[0]$-$C_\alpha[N-1]$, of a multi-bit control value, C_α (or, control value $/C_\alpha$). Each of the control transistors 437_0-437_{N-1} has a binary weighted gain such that a current of $I_{REF} \times 2^i$ (where i represents the i^{th} transistor in the positions 0, 1, 2, …, N-1) flows through control transistor 437_i when the corresponding control signal component is high. Thus, if all the constituent bits of the control value $C_\alpha[N-1:0]$ are high, then I_{REF} flows through control transistor 437_0, $I_{REF}x2$ flows through transistor 437_1, $I_{REF}x4$ flows through control transistor 437_2, and so forth to control transistor 437_{N-1} which conducts $I_{REF}x2^{N-1}$. Accordingly, control transistors 437_0-437_{N-1} are designated x1, x2…, $x2^{N-1}$ transistors, respectively. By this arrangement, the control value $C_\alpha[N-1:0]$ may be set to any of 2^N values to select bias currents that range from 0 to $I_{REF}x2^{N-1}$ in increments of I_{REF}. The biasing transistors 439_0-439_{N-1} have gate terminals coupled to receive a bias voltage, ~~VBIAS~~ V_{BIAS}, that is adjusted as necessary (e.g., by a biasing circuit) to establish or maintain a desired I_{REF}.

[0046] The adaptive module 503 receives the error sample

from the level sampler 501 and data samples D_{N-1} and D_{N-2} from the partial response receive circuit 200 and, in response, generates control values, C_α and $/C_\alpha$, to establish the $\pm\alpha$ levels within the partial response receive circuit 200, and the control value, C_{DLEV}, to establish the data level threshold within the level sampler 501. In one embodiment, the adaptive module 503 initially updates the C_{DLEV} value upon detecting reception of the $1+\alpha$ data pattern (i.e., D[N-1:N-2]=11) until the comparator 507 indicates that the data level threshold matches the $1+\alpha$ data level. Thereafter, the adaptive module 503 updates the C_{DLEV} value in response to the $1-\alpha$ data pattern (10) until the D_{LEV} threshold matches the $1-\alpha$ data level. The control value, $C\alpha$, may be generated, for example, by halving the difference between the two C_{DLEV} values (i.e., $C_{1+\alpha}$ and [[$C_{1-\alpha}$]] $\underline{C_{1-\alpha}}$), and the $/C\alpha$ control value may be generated by complementing the C_α value.

[0047] Figure 21 illustrates the operation of the adaptive module 503 of Figure 20 according one embodiment. Initially, at block 521, the control values, C_α and C_{DLEV}, and an internally maintained control value, $C_{2\alpha}$, are each set to a nominal zero value. In one embodiment, the nominal zero value corresponds to a DAC midpoint value. For example, in an 8-bit DAC, a midpoint value of 1000 0000b (the 'b' indicating binary notation) or 128 decimal may be used as the nominal zero value. The $C_{-\alpha}$ value may be generated by subtracting the C_α value from the full-scale DAC value. Thus, in the eight-bit example, when $C_{+\alpha} = 128$, $C_{-\alpha} = (2^8-1) - 128 = 127$. [[ ]] It will be appreciated that this result may be obtained by complementing C_α (i.e., $/C_\alpha = C_{-\alpha}$).

[0050] If, at decision block 523, the upper data level is deemed to be found, the history of increment and decrement operations is cleared and a second level adapting loop is begun at decision block 535. At decision block 535, the history of increment and decrement operations is evaluated to determine whether a data level threshold corresponding to the 1-α data level has been found (i.e., LOWER DLEV FOUND). In one embodiment, if, over the last N updates to the C_{DLEV} value, the difference between the number of increment operations and the number of decrement operations is less than a predetermined value, the data level threshold is deemed to be dithering about the 1-α signal level and the lower data level threshold is therefore considered found. If the lower data level threshold has not been found, then the sample values generated by the partial response receive circuit, D[N-1:N-2], are evaluated in decision block 537 to determine whether a signal level at the 1-α level has been received. If not, decision block 537 is repeatedly entered for subsequent sample value pairs until a signal level at the 1-α level has been received. When data samples that correspond to the 1-α level are detected, the error sample generated by the level sampling circuit, E_{DLEV}, is evaluated at decision block 539 to determine whether the incoming signal level is above or below the data threshold level established by the present value of C_{DLEV}. If the error sample is a '0', as it will be initially, the signal level is below the data threshold level, and the C_{DLEV} value is decremented at 543 to decrease the DLEV threshold level, and the $C_{2\alpha}$ control value is incremented to track the difference between the upper and lower data level thresholds. If the

error sample is determined to be a '1' at decision block 537, then C_{DLEV} is incremented and $C_{2\alpha}$ decremented at block 541. By this arrangement, when the data level threshold reaches the ~~1-~~ ~~α~~ 1-α data level, the control value, $C_{2\alpha}$, will be representative of twice the +α threshold level. Accordingly, at block 545, the C_{α} value is generated by dividing $C_{2\alpha}$ by 2 (e.g., by right shifting or otherwise dropping the least significant bit of $C_{2\alpha}$). The $C_{-\alpha}$ value may be generated by complementing the C_{α} value. Thereafter, the process is repeated starting at decision block 523. Alternatively, an updated $C_{2\alpha}$ value may be generated by counting the return increments from the lower data level threshold to the upper data level threshold, and another updated value of $C_{2\alpha}$ generated on a subsequent return to the lower data level threshold, and so forth. The C_{α} value may be updated after each regeneration of the $C_{2\alpha}$ value. Also, rather than finding the 1+α and 1-α data levels, the 1+α and [[-]] [[1+α]] -1+α data levels may be determined, and the corresponding data level control values averaged to generate the C_{α} value.

[0055] Still referring to Figure 22, when the mode select signal 572 is high, the dual mode receiver 550 is switched to the partial response mode. In the partial response mode, the comparators 553 and 555 are used to compare the incoming data signal against the partial response threshold levels +α and ~~-~~ ~~α~~ -α, respectively. The samples values generated by the comparators 553 and 555 are buffered in storage circuits 554 and 556, respectively, then provided to select circuit 563 which selects one of the samples according to the state of the

previously received sample. That is, one of the D_{N-1} samples stored in storage circuits 554 and 556 is selected to be stored in storage circuit 567 according to the D_{N-2} sample previously stored in the storage circuit 567. The D_{N-2} sample is stored in the storage circuit 578 to generate the D_{N-3} sample value. During a given symbol time, both the D_{N-2} and ~~D_{N-3}~~ $\underline{D_{N-3}}$ samples are provided to the adaptive module 581 via select circuits 579 and 575, respectively. Thus, in 4-PAM mode, the adaptive module 581 receives the MSB/LSB pair for each incoming 4-PAM symbol, and in partial response mode, the adaptive module 581 receives the D[N-2:N-3] sample values that represent one of the four states of the bimodal signal illustrated in Figure 4.

[0075] Still referring to Figure 28, when the partial response receiver 700 is operated in the partial response mode, the transitions of interest are as shown in Figure 30. That is, a partial response state transition from 10-to-01 or 10-to-01 crosses the zero threshold level at the desired edge clock transition time, T1; a state transition 11-to-01 crosses the $+\alpha$ threshold level at T1; and a state transition from 00-to-10 crosses the [[$-\alpha$]] $\underline{-\alpha}$ threshold level at T1. Enumerating the partial response mode transitions that cross the zero, $+\alpha$ and $-\alpha$ threshold levels at T1 as transition types (1), (2) and (3), respectively, it can be seen that type (1) transitions are those in which the current data sample, D_N, does not match the immediately preceding data sample, D_{N-1}, which, in turn, does not match the twice-removed data sample, D_{N-2} (i.e., (D_N xor D_{N-1}) & (D_{N-1} xor D_{N-2})); type (2) transitions are those in which the current data sample, D_N, is low, and

the two immediately preceding data samples, D_{N-1} and D_{N-2}, are high (i.e., $/D_N$ & D_{N-1} & D_{N-2}); and type three (3) transitions are those in which the current data sample, D_N, is high, and the two immediately preceding data samples, D_{N-1} and D_{N-2}, are low (i.e., D_N & $/D_{N-1}$ & $/D_{N-2}$). Thus, in one embodiment, when the mode select signal 712 selects a partial response mode of operation within the partial response receiver 700, the clock recovery circuit 705 adjusts the phase of the edge clock and sampling clock signals 610, 210 in response to the data and transition samples generated by circuit 701 and comparators 707, 708, 709 in accordance with the following table:

D[N-1:N-2]	D[N:N-1]	Center Time Crossing At:	$T_N(+\alpha)$	$T_N(-\alpha)$	$T_N(0)$	Early/Late Count Adj.
00	10	$-\alpha$	X	0/1	X	+1/-1
01	00	--	X	X	X	--
01	10	0	X	X	0/1	+1/-1
10	01	0	X	X	0/1	-1/+1
10	11	--	X	X	X	--
11	01	$+\alpha$	0/1	X	X	-1/+1

Table 2

[0076] Still referring to Figure 30, if the $+\alpha$ and ~~$-\alpha$~~ $\underline{-\alpha}$ threshold levels are initially set to zero as indicated by reference numeral 741, it can be seen that the edge clock alignment will initially converge to a point that is phase delayed relative to the desired edge sampling point, T1. As the levels of $\pm\alpha$ progress toward their ultimate setpoints at 742 and 743, however, the edge clock phase alignment will

converge to the desired sampling point, T1.

[0078] The transition detect circuit 725 includes a set of combinatorial logic circuits 727_1, 727_2 and 727_3 that generate type (1), type (2) and type (3) transition detect signals 730 for both 4-PAM and partial response data states in accordance with the type (1), type (2) and type (3) transition types described in reference to Figures 29 and 30. In the embodiment of Figure 31, combinatorial logic circuit 727_1 generates a 4-PAM type (1) transition detect signal 730_{1A} and a 2-PAM, partial response type (1) transition detect signal 730_{1B} as follows:

Signal 730_{1A} = (MSB_N xor MSB_{N-1}) & (LSB_N xnor LSB_{N-1}); and

Signal 730_{1B} = (D_N xor D_{N-1}) & (D_{N-1} xor D_{N-2}).

Similarly, combinatorial logic circuits 727_2 and 727_3 generate 4-PAM type (2) and type (3) transition detect signals 730_{2A} and 730_{3A}, and 2-PAM, partial response type (2) and type (3) transition detect signals, 730_{2B} and 730_{3B}, as follows:

Signal 730_{2A} = (MSB_N & MSB_{N-1}) & (LSB_N xor LSB_{N-1});

Signal 730_{3A} = (/MSB_N & /MSB_{N-1}) & (LSB_N xor LSB_{N-1});

Signal 730_{2B} = /D_N & D_{N-1} & D_{N-2}; and

Signal 730_{3B} = D_N & /D_{N-1} & /D_{N-2}.

It should be noted that, in both partial response mode and 4-PAM mode, two successive pairs of data samples are used within the transition detect circuit 725 (e.g., MSB/LSB_N and ~~MSB/LSB_{N-1}~~ MSB/LSB_{N-1} in 4-PAM mode; D_N/D_{N-1} and D_{N-1}/D_{N-2} in partial response mode) to generate the transition detect signals 730. One or more of the data sample pairs may be buffered within a storage circuit within transition detect circuit 725 or elsewhere within the dual mode receiver and made available to

the various combinatorial logic circuits 727. Also, the latency of the data samples referred to in Figure 31, though depicted as N, N-1 and N-2, may be any latency necessary to match the latency of the data samples output from the data receive and level sampling circuit 701 of Figure 28.

[0086] Figure 35 illustrates a partial response receiver 800 that operates in accordance with the partial response states shown in Figure 34. Four comparators 801_1, 801_2, 801_3 and 801_4 are provided to compare the signal level of an incoming symbol, D_N, against the four partial response threshold levels $\alpha+\beta$, $\alpha-\beta$, $-\alpha+\beta$ and $-\alpha-\beta$, respectively. The outputs of each of the comparators 801 are stored in a first stage of storage circuits 802_1-802_4 (e.g., in response to a sampling clock signal, not shown), with the sample values that correspond to the $+\alpha$ threshold levels (i.e., $D_{N-1}(\alpha+\beta)$ and ~~$D_{N-1}(\alpha-\beta)$~~ $\underline{D_{N-1}(\alpha-\beta)}$) being supplied to a first select circuit 810 and the sample values that correspond to the $-\alpha$ threshold levels (i.e., $D_{N-1}(-\alpha+\beta)$ and $D_{N-1}(-\alpha-\beta)$) being supplied to a second select circuit 812. Each of the first and second select circuits 810 and 812 selects between its respective pair of input samples according to the state of a previously resolved sample value, D_{N-3}, stored in storage circuit 820. More specifically, if the resolved sample value, D_{N-3}, is a '1', then β, the partial response to D_{N-3}, is a positive value and the select circuits 810 and 812 select the sample values [[$D_{N-1}(\alpha+\beta)$]] $\underline{D_{N-1}(\alpha+\beta)}$ and $D_{N-1}(-\alpha+\beta)$, respectively, that correspond to the positive β state. If the D_{N-3} sample is a logic '0' value, then β is a negative value and the select circuits 810 and 812 select the sample values $D_{N-1}(\alpha-\beta)$ and $D_{N-1}(-\alpha-\beta)$ that correspond to the negative β state. The D_{N-1} sample values

selected by the select circuits 810 and 812 correspond to the $+\alpha$ and $-\alpha$ partial response states, respectively, and are stored in storage circuits 814 and 816 to provide D_{N-2} sample values $D_{N-2}(\alpha)$ and $D_{N-2}(-\alpha)$. The $D_{N-2}(\alpha)$ and $D_{N-2}(-\alpha)$ samples are output from the storage circuits 814 and 816 to respective inputs of select circuit 818. The state of the D_{N-3} sample value indicates the sign of the partial response contribution in the D_{N-2} signal. That is, if $D_{N-3}=1$, α is positive, and if $D_{N-3}=0$, α is negative. Accordingly, the D_{N-3} sample value is supplied to a select input of select circuit 818 to select either $D_{N-2}(+\alpha)$ or $D_{N-2}(-\alpha)$. Thus, the partial response receiver 800 of Figure 35 simultaneously compares the incoming data signal against four different partial response thresholds, then selects one of the four sample values to be the output sample value (D_{N-3}) based on the previously resolved state of the α and β partial response components. Partial response components from more than two previously received symbols may be accommodated in a similar manner by increasing the number of comparators to match the number of partial response levels to be resolved, and then selecting the desired partial response sample on the basis of the partial response components indicated by a previously resolved sample value.

[0090] Figure 38 illustrates a 4-PAM partial response receiver 875 according to an embodiment of the invention. The receiver 875 includes four 4-PAM receive circuits 877_1-877_4 (i.e., each capable of resolving the signal level of an incoming symbol into one of four possible two-bit combinations) each having a threshold level that is offset according to one of the four partial response levels (3α, α, -

~~α,~~ -α, or -3α). In the case of receive circuit 877_4, for example, the 3α offset (corresponding to a prior symbol level of 10) is applied to each of the internal levels generated to resolve the 4-PAM signal. That is, instead of comparing the incoming signal with levels of -2, 0, and 2, the incoming signal is compared with -2+3α, 3α and 2+3α (i.e., the threshold values between the 3+3α, 1+3α, -1+3α, -3+3α constellation depicted in Figure 37). Similarly, 4-PAM receive circuit 877_3 compares the incoming signal with thresholds offset by α (i.e., -2+α, α and 2+α), comparator 877_2 compares the incoming signal with thresholds offset by -α (i.e., -2-α, -α, and 2-α) and comparator 877_1 compares the incoming signal with thresholds offset by -3α (i.e., -2-3α, -3α and 2-3α). By this arrangement, the incoming signal is resolved into four 2-bit sample values according to each of the four possible partial responses to the preceding symbol. The preceding symbol, MSB/LSB[N-1], having been selected according to the state of MSB/LSB[N-2], is stored in storage element 881 and applied to the select input of select circuit 879 to select the one of the four sample values generated in accordance with the incoming signal level. While the partial response operation has been described in terms of a 4-PAM receiver that enables partial response selection based on a single preceding symbol, the circuits and operation described may be extended to other PAM levels (e.g., 8-PAM, 10-PAM, etc.) and/or to include the partial response to additional preceding bits.

[0094] In the embodiment of Figure 39, each partial response receiver 887 includes a partial response receive

circuit 888, level sampler 889, adaptive module 890, edge sampler 891 and clock data recovery circuit 892. The partial response receive circuit 888 may be a multi-mode receive circuit as described above (i.e., capable of being switched between a multi-level signaling mode and a partial response mode), or may be dedicated to partial response operation. Also, the partial response receive circuit may operate on incoming binary or multi-level signals (e.g., 2-PAM, 4-PAM, 8-PAM, 10-PAM, etc.) having any data rate (e.g., single data rate, double data rate, quad data rate, octal data rate, decade data rate, etc.). Thus, the partial response receive circuit 888 may be implemented by any of the partial response receive circuit embodiments described herein. Similarly, the level sampler 889 and adaptive module 890 may be implemented by any of the level sampler and adaptive module embodiments described herein. For example, though depicted as outputting a single error sample, E_{DLEV}, the level sampler 889 may output multiple error samples to the adaptive module 890, and the adaptive module 890 may output any number of control values to the level sampler 889, partial response receive circuit 888 and edge sampler 891 (e.g., as shown in Figures 14, 28 and 36) in addition to or instead of C_{DLEV}, [[$C_{\square}$, /$C_{\square}$]] $C\alpha$, /$C\alpha$, and C_0. Also, though depicted in Figure 39 as recovering a sample clock signal (SCLK) and edge clock signal (ECLK), the edge sampler 891 and clock data recovery circuit 892 may recover any number of clock signals as described above in reference to Figures 24 and 26 (e.g., for use in multi-data rate embodiments). Further, the edge sampler 891 and clock data recovery circuit 892 may recover phase information (i.e., for adjusting the phase of the recovered clock signals) from any

or all transitions of the incoming data signal 893 as described above. The edge sampler 891 and clock data recovery circuit 892 may be omitted from the partial response receiver 887 in an embodiment in which clock signals, strobe signals or other timing signals are provided by another source, such as an external or internal clock generator, or separate clock recovery circuit.

[0095] Figure 40 illustrates an input circuit 895 according to an alternative embodiment of the invention. The input circuit 895 is similar to the input circuit 885 of Figure 39 (and may be implemented in all the alternative embodiments described in reference to Figure 39), except that the circuitry used to generate partial response thresholds (or representative control values) and sampling clock signals is shared among multiple partial response receive circuits 888_1-888_M. That is, a single level sampler 889 and corresponding adaptive module 890 are used to generate control values [[$C_{\square}$, $/C_{\square}$]] $C\alpha$, $/C\alpha$, and C_0 (and additional or different threshold control values in multi-level signaling embodiments and embodiments that do not include clock recovery circuitry) that are supplied to each of the partial response receive circuits 888_1-888_M, and a single edge sampler 891 and corresponding clock data recovery circuit 892 are used to generate the sampling clock signal (SCLK) that is supplied to each of the partial response receive circuits 888_1-888_M. Multiple sampling clock signals may be generated and shared among the partial response receive circuits 888_1-888_M in multi-data rate embodiments. By sharing the circuitry for generating control thresholds and/or the circuitry for generating sampling clock

signals, the amount of circuitry within the input circuit 895 is substantially reduced relative to input circuit 885, reducing production and operational cost of the host integrated circuit device (i.e., due to reduced die area consumption, layout complexity, test and verification time, power consumption, etc.). Note that, in an embodiment in which the sampling clock signal is provided by circuitry other than clock data recovery circuitry (e.g., external clock source, internal clock generated), the edge sampler 891 and clock data recovery circuit 892 may be omitted. Alternatively, programmable selection of the clock source may be used to select either the recovered sampling clock (i.e., recovered by operation of the edge sampler 891 and clock data recovery circuit 892) or another clock source to provide a sampling clock signal to the partial response receive circuits 888_1-888_M. As in the embodiment of Figure 39, the signal lines 893_1-893_M may be used to deliver distinct serial transmissions, or transmission of related groups of bits (e.g., the M bits received during a given symbol time representing one or more multi-bit digital values) as, for example, in the case of a parallel bus or any other signaling system in which the threshold control values and/or timing control signals are expected to be substantially similar (e.g., substantially same thresholds and/or clock phases) across multiple signaling paths. Also, while a single level sampler 889 and corresponding adaptive module 890 are depicted in Figure 40 as generating threshold control values [[$C_{\square}$, /$C_{\square}$]] $C\alpha$, /$C\alpha$ and C_0 for each of the partial response receive circuits 888_1-888_M, in an alternative embodiment, multiple level sampler/adaptive module pairs may be used to generate threshold control values

for respective subsets of the partial response receive circuits 888_1-888_M. Respective edge sampler/clock data recovery circuit pairs may similarly be used to generate sampling clock signals for corresponding subsets of partial response receive circuits 888_1-888_M.

[0097] Figure 41 illustrates a signaling system 950 having a transmit device 951 and receive device 953 coupled to one another via a signaling path 122. The transmit device 951 includes an equalizing transmit circuit 957 and tap control logic 955, and the receive device 953 includes a partial response receive circuit 971 (which may, for example, be a multi-mode circuit or any other of the partial response receive circuits disclosed herein), level sampler 973 and adaptive module 975. Both the transmit device 951 and receive device 953 may include numerous other circuits not shown in Figure 41 (e.g., application logic, additional transmit circuits and/or receive circuits, etc.). The equalizing transmit circuit 957 includes a number of output drivers 961_0-961_{N-1} to drive a symbol onto signaling path 122 in response to a transmit timing signal (not shown) and in accordance with a set of weighting values W_0-W_{N-1} and the state of data values D_0-D_{N-1}. Each of the data values D_0-$D_{-(N-1)}$ is stored within a shift register 959 (or similar storage circuit) and includes a number of constituent bits in accordance to the number of bits encoded into each symbol transmission on the signaling path 102. For example, in a 4-PAM system, each of the data values, D_0-$D_{-(N-1)}$, includes two constituent bits. More generally, in a M-PAM system, each of the data values includes $\log_2(M)$ constituent bits. After each symbol transmission, the

contents of the shift register 959 are shifted forward so that a new data value is shifted into position D_0, and the data value at position $D_{-(N-1)}$ is overwritten by the data value previously at position $D_{-(N-2)}$.

[0105] Figure 45 depicts some of the signal transition types to be expected from an embodiment of sampler 1005 that supports 2PAM and 4PAM communication schemes. From left to right:

a. the first transition type T2P/4Pa represents either a 2PAM transition from one to zero or a 4PAM transition from 10 to 00;
b. the second transition type T4Pa represents a 4PAM transition from 11 to 00;
c. the third transition type T4Pb represents a 4PAM transition from 10 to ~~10~~ 01 ;
d. the fourth transition type T4Pc represents a 4PAM transition from 10 to 11;
e. the fifth transition type T4Pd represents a 4PAM transition from 11 to 01; and
f. the sixth transition type T4Pe represents a 4PAM transition from 01 to 00.

The foregoing transitions are not exhaustive. For example, an opposite transition type exists between any two logic levels. Further, as discussed above, some transition types take place at non-ideal voltages and times. The following discussion illustrates one embodiment using the relatively simple transition types illustrated in Figure 45, but this embodiment can be extended to sense any number of transition types using, e.g., circuits and methods of the types detailed above.

[0114] Figure 46 depicts transition analyzer 1050 in accordance with one embodiment. Analyzer 1050 includes a 64-bit FIFO buffer 1060 connected to transition-type input terminals T2P/4Pa and five six-bit counters 1062 connected to respective transition-type input terminals T2P(+α), T4Pb, T4Pc, T4Pd, and T4Pe. Counters 1062 each produce a six-bit ~~numbers~~ number indicative of the number of detected transition-type input signals on the corresponding input node.

[0118] Figure 47 details an embodiment of transition select logic 1020. Control signals TS[5:0] from control circuit 1015 connect to select logic 1020 ~~and~~ on like-named lines. The LSB, TS(0), controls a multiplexer 1100 and each of the remaining bits TS[5:1] connects to one input of a respective one of a collection of two-input AND gates. The second input of each AND gate connects to a line from transition detector 1010 associated with one of the transition types.